

FIG.1

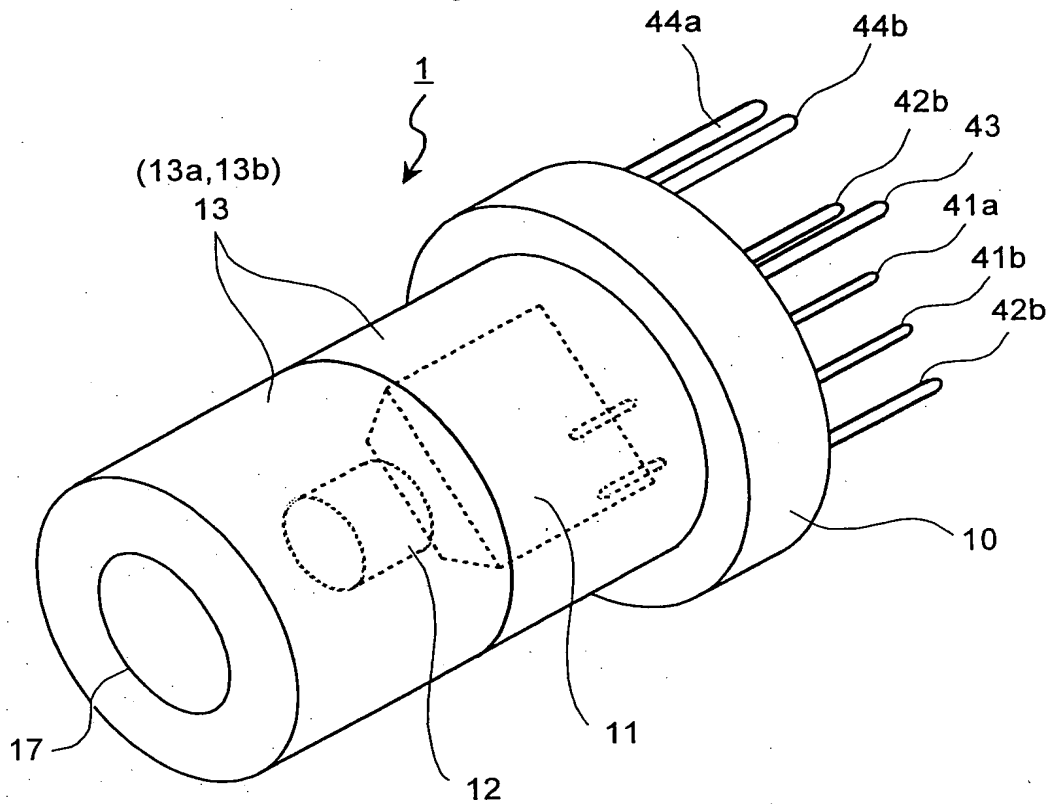
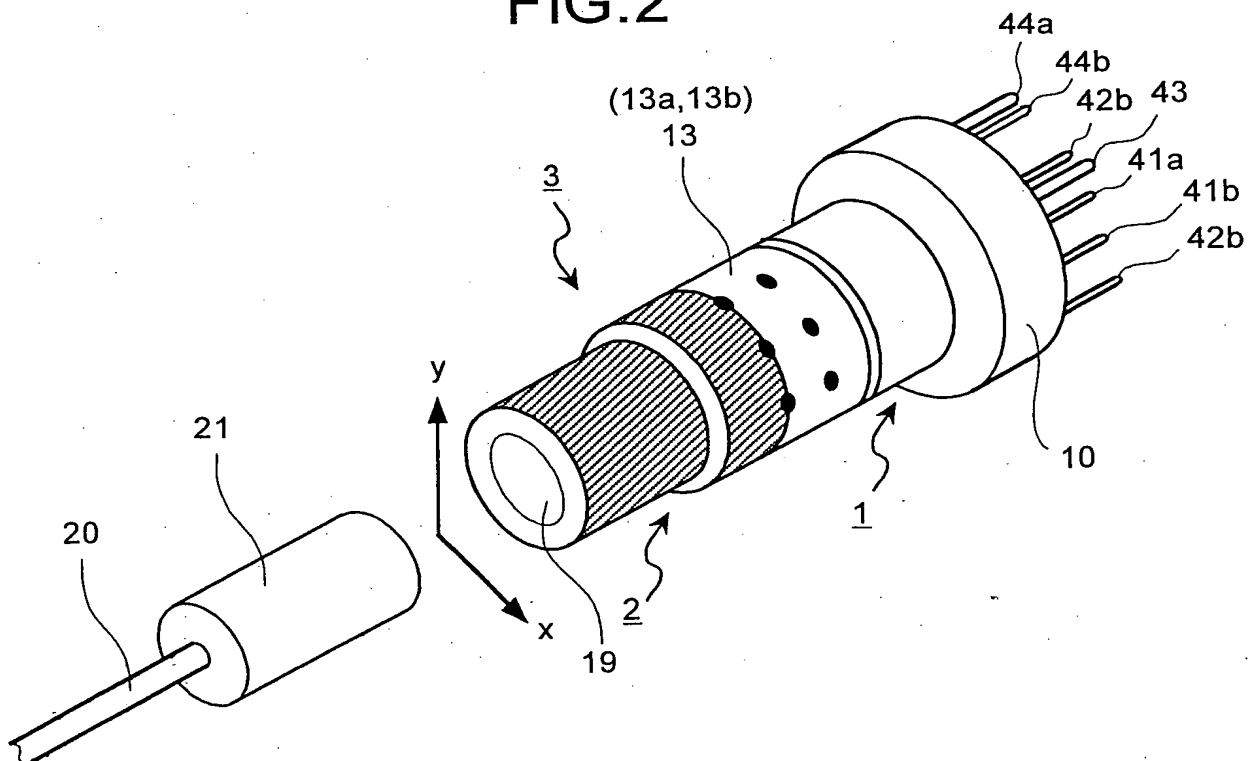


FIG.2



APPLN. FILING DATE: JULY 1, 2004

TITLE: OPTICAL SEMICONDUCTOR PACKAGE (AS AMENDED)

INVENTOR(S): HIROSHI ARUGA ET AL.

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This cross-sectional view shows a semiconductor device with a central cavity. A central electrode, labeled 40, is positioned within the cavity. The electrode is connected to a lead, labeled 50, which passes through a series of layers. The layers are labeled 41a, 41b, 44a, 44b, and 43. The device is mounted on a substrate, labeled 10, and is surrounded by a protective layer, labeled 15. The central cavity is defined by a central region, labeled 11, and is surrounded by a layer, labeled 12. The device is also surrounded by a layer, labeled 13a, and a layer, labeled 13b. The device is shown in a cross-sectional view, with a central region, labeled 11, and a central electrode, labeled 40, positioned within the cavity. The electrode is connected to a lead, labeled 50, which passes through a series of layers. The layers are labeled 41a, 41b, 44a, 44b, and 43. The device is mounted on a substrate, labeled 10, and is surrounded by a protective layer, labeled 15. The central cavity is defined by a central region, labeled 11, and is surrounded by a layer, labeled 12. The device is also surrounded by a layer, labeled 13a, and a layer, labeled 13b.

FIG. 4

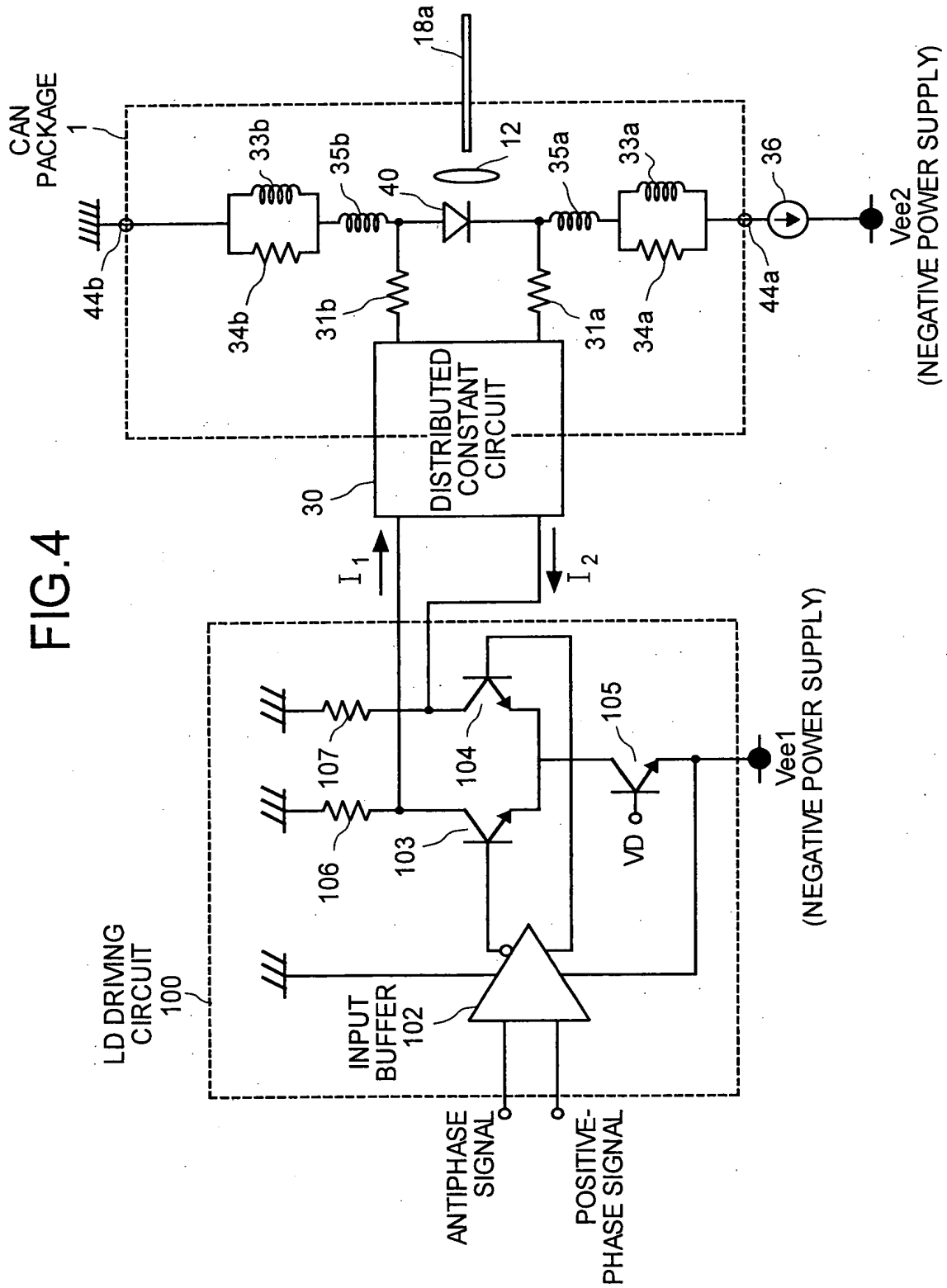


FIG.6

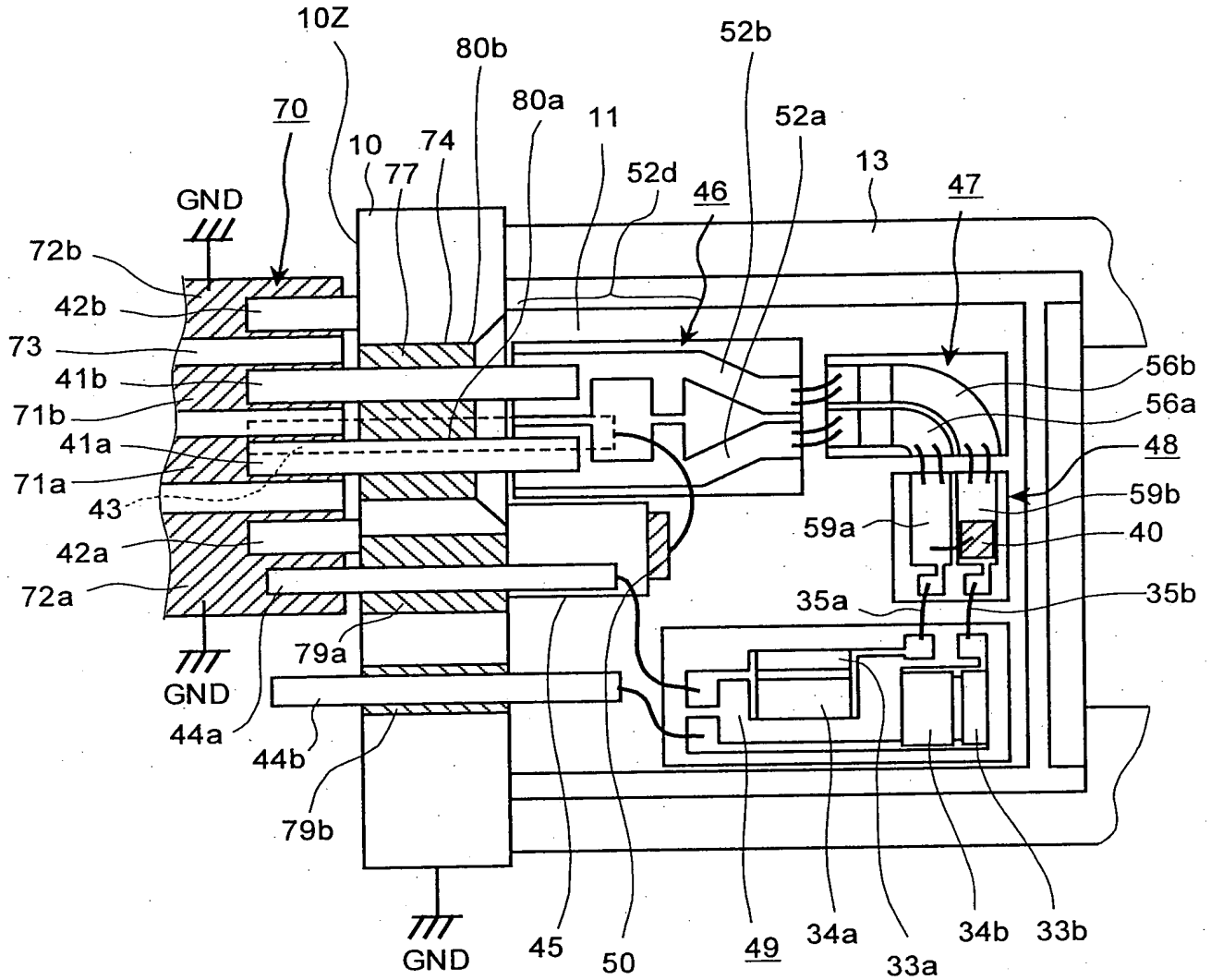


FIG. 7

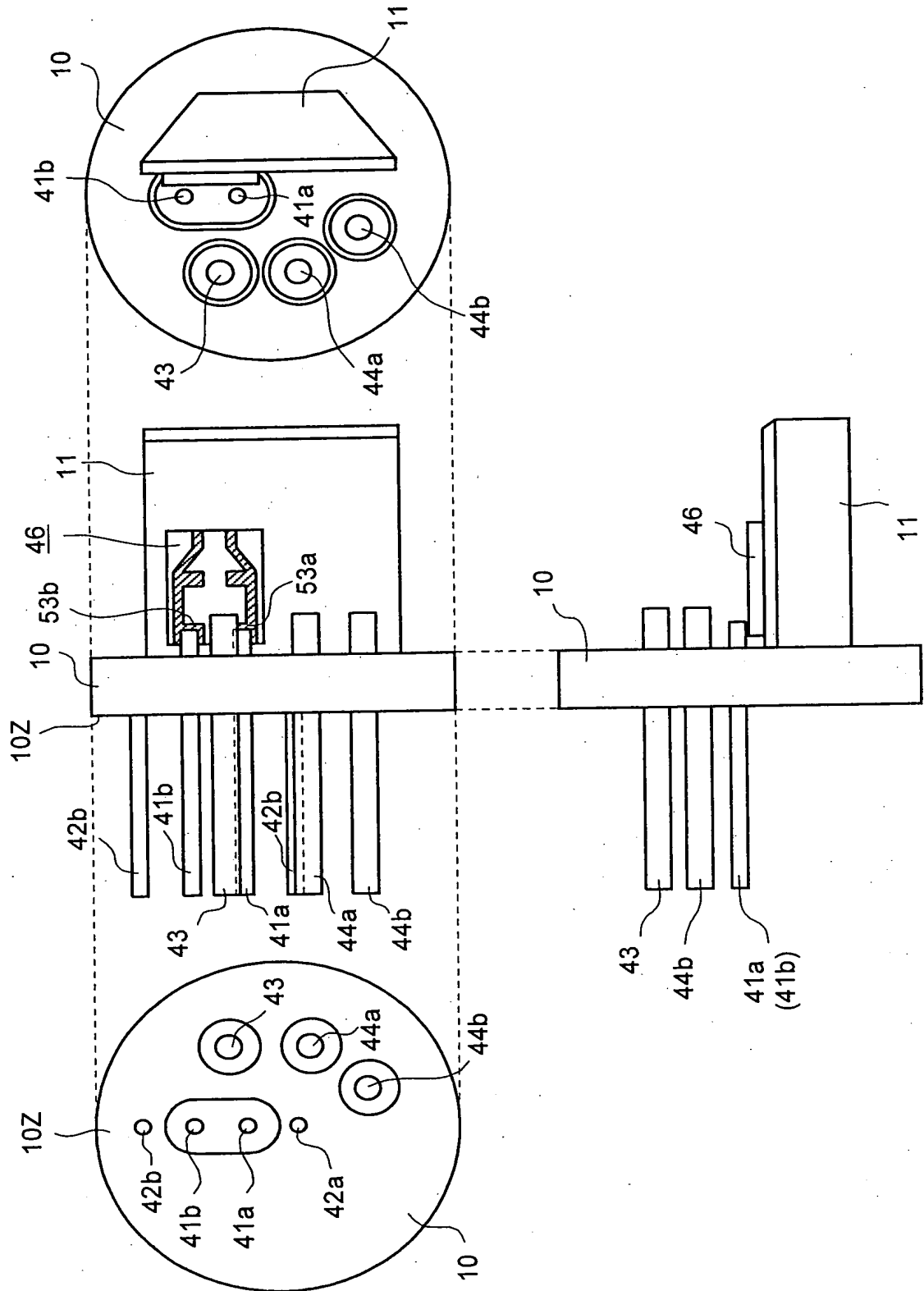


FIG. 8

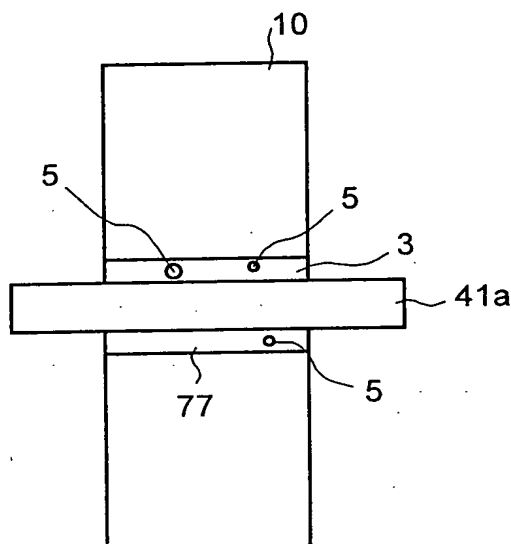


FIG. 9

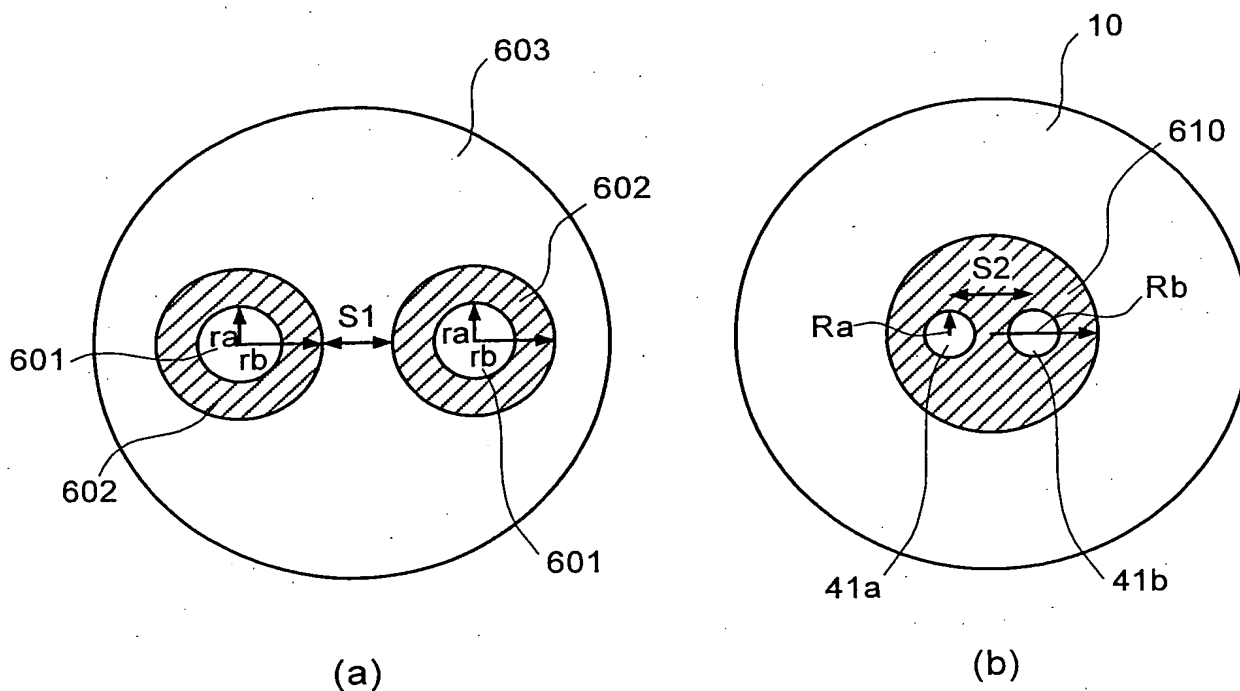


FIG.10A

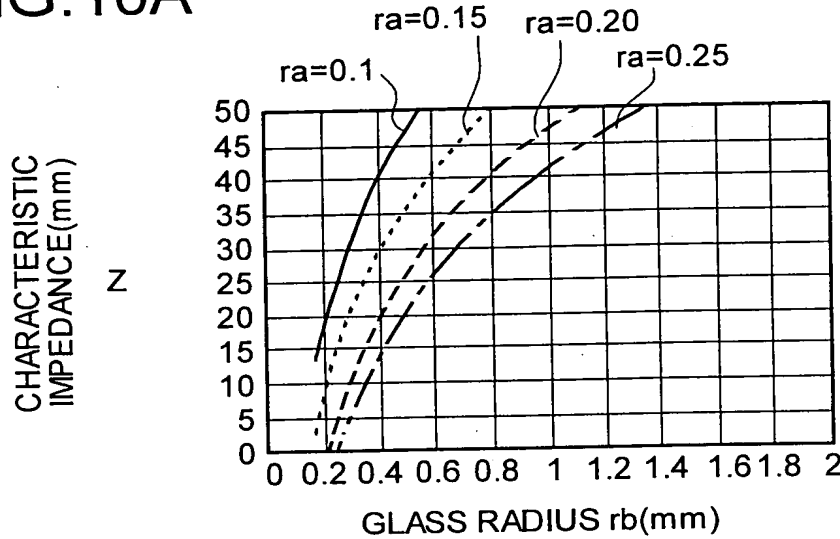


FIG.10B

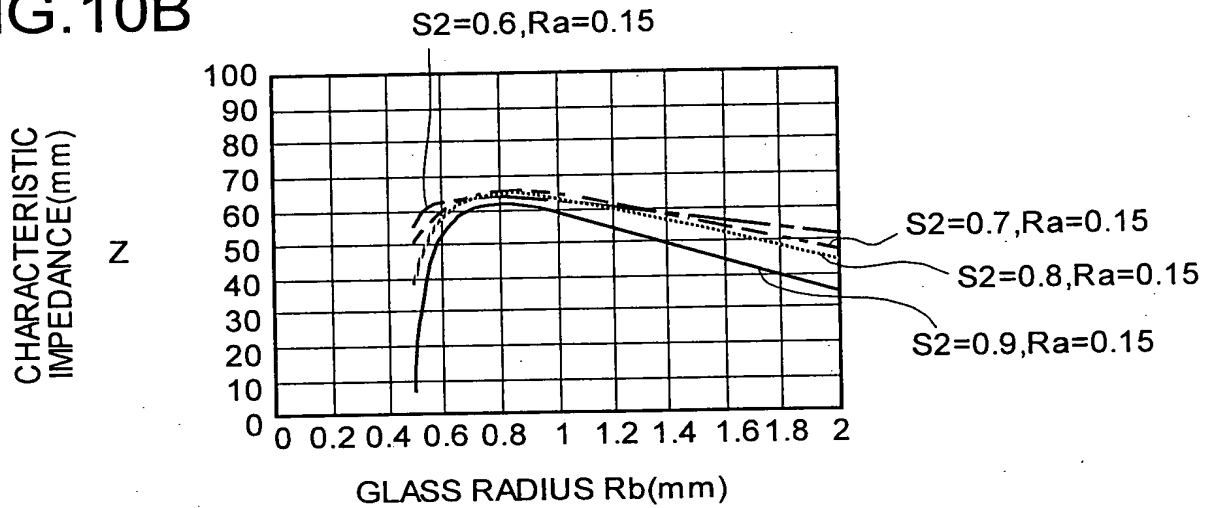


FIG.10C

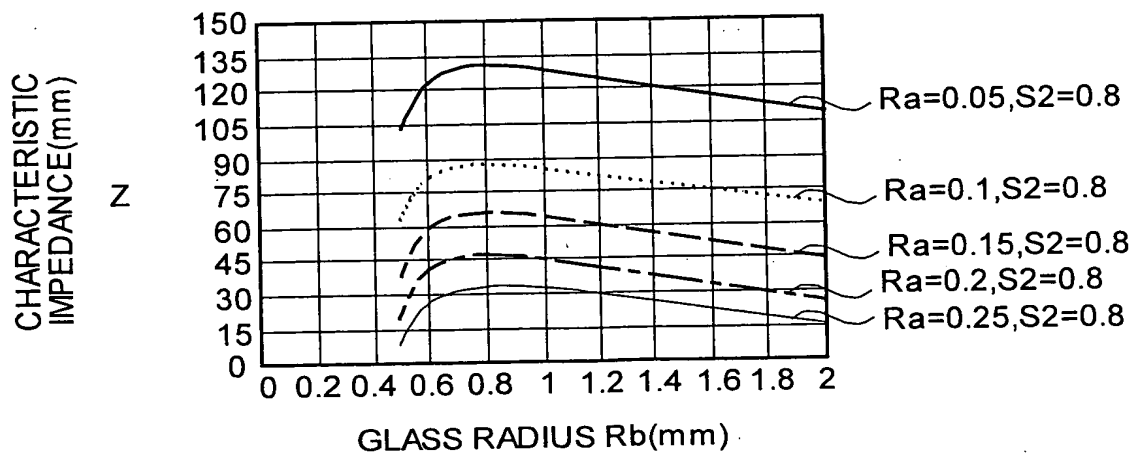


FIG. 11

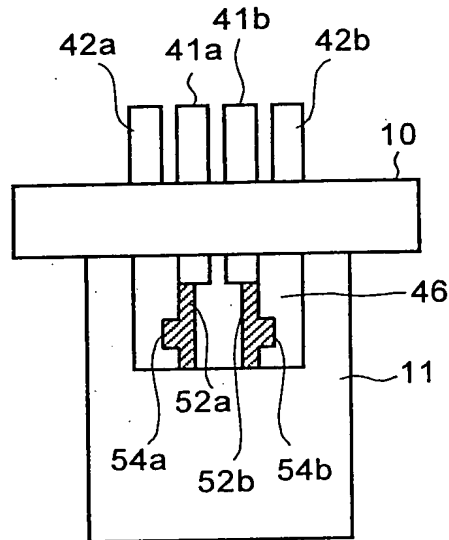


FIG. 12

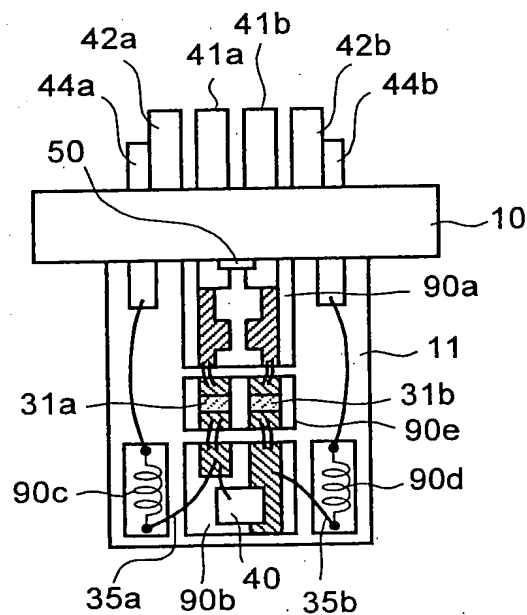


FIG. 13

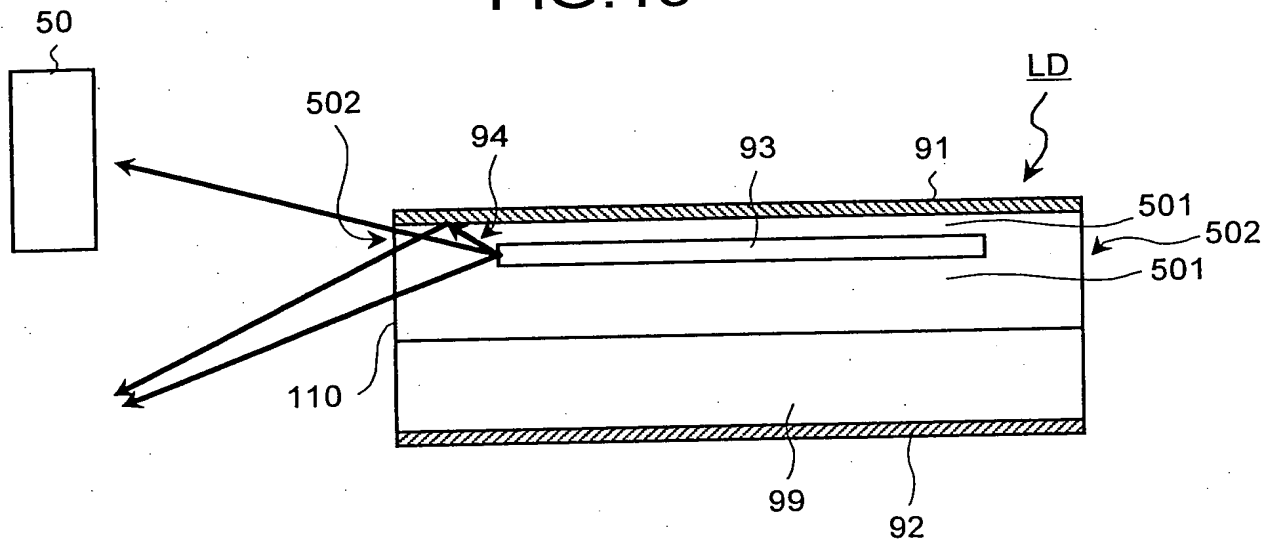
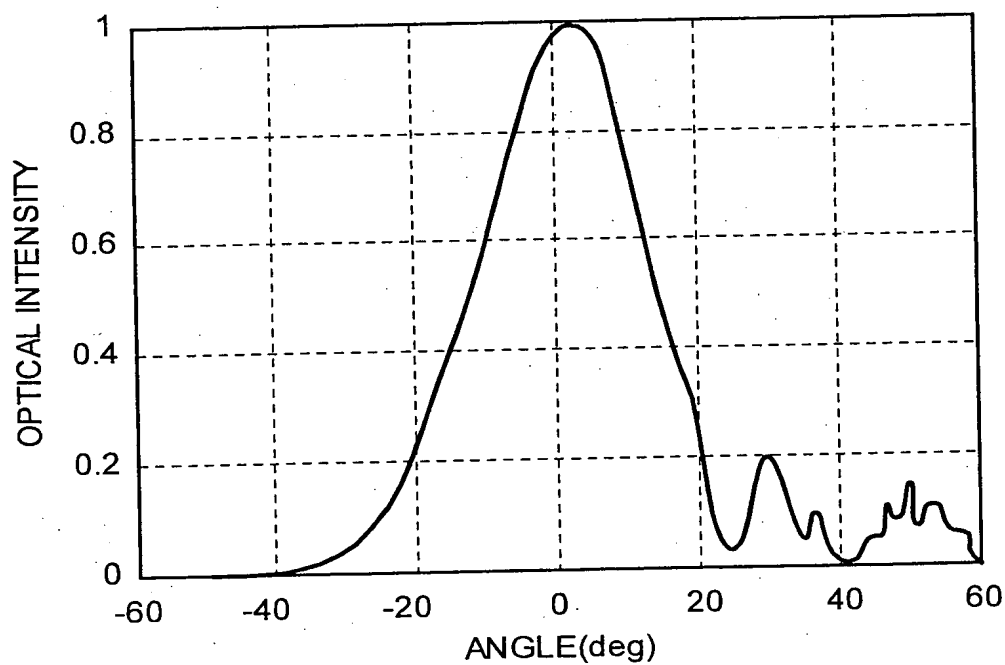


FIG. 14



→ SEMICONDUCTOR SUBSTRATE SIDE

FIG. 15

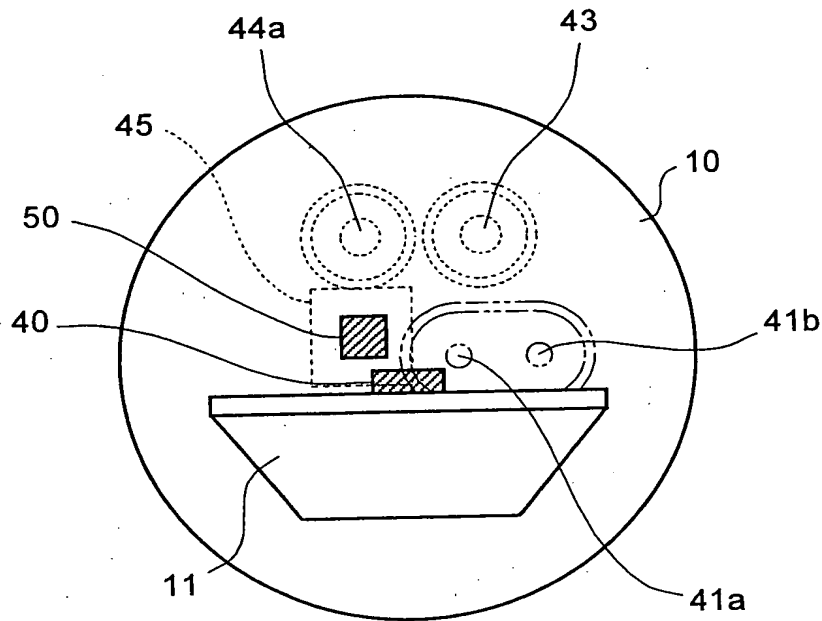


FIG. 16

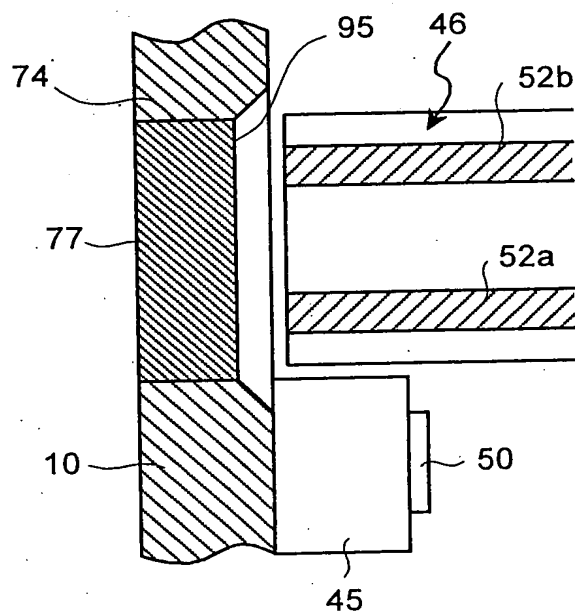


FIG. 17

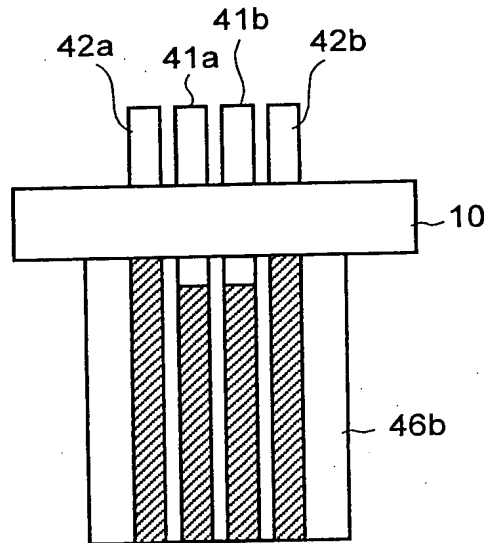
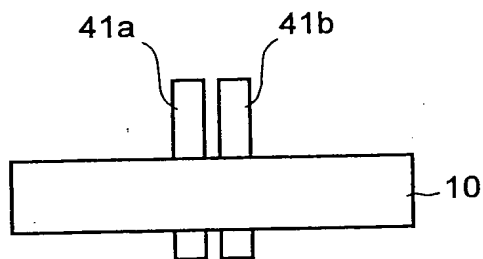


FIG. 18



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FIG. 19A

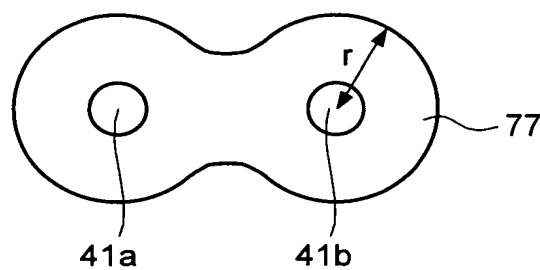


FIG. 19B

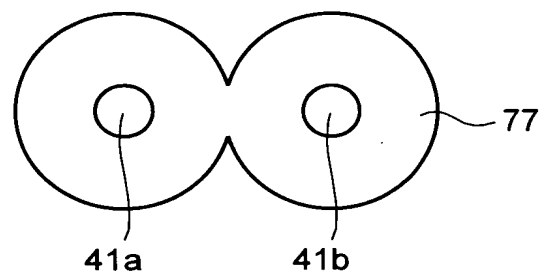


FIG. 19C

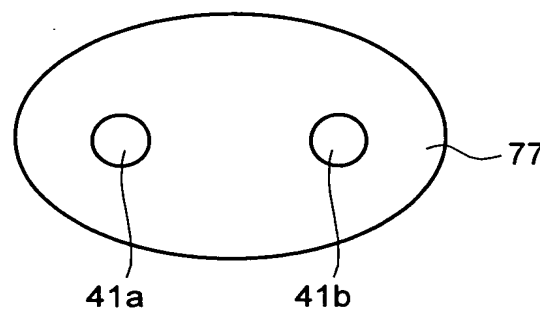


FIG. 20

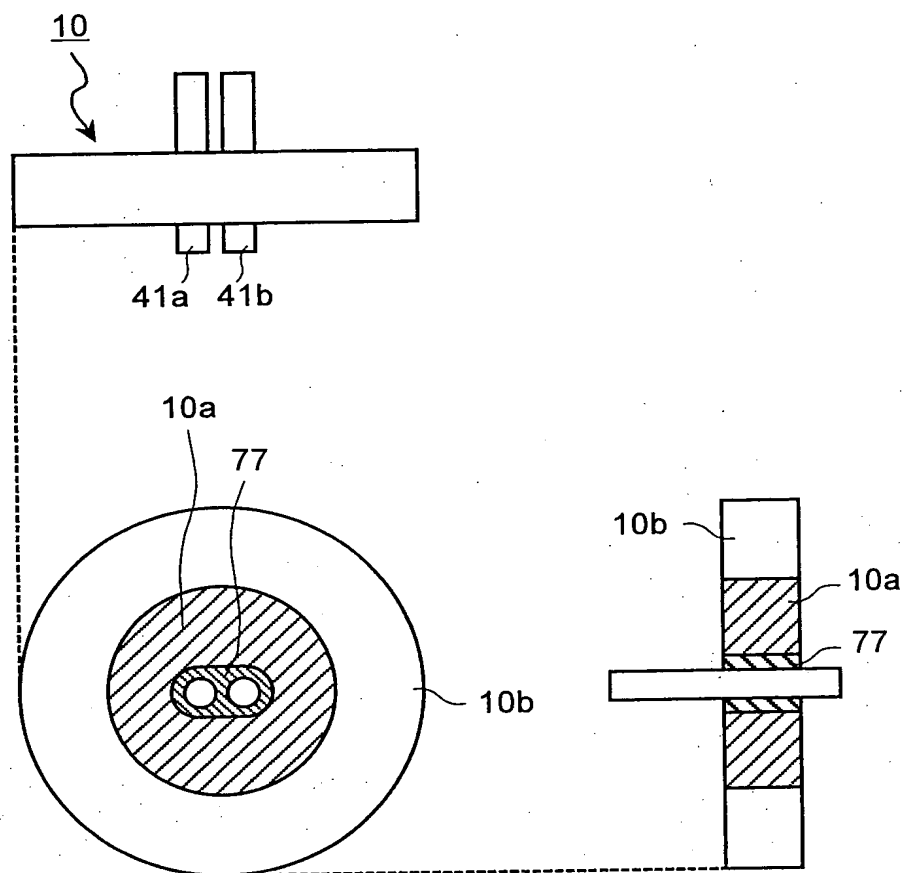


FIG.21B

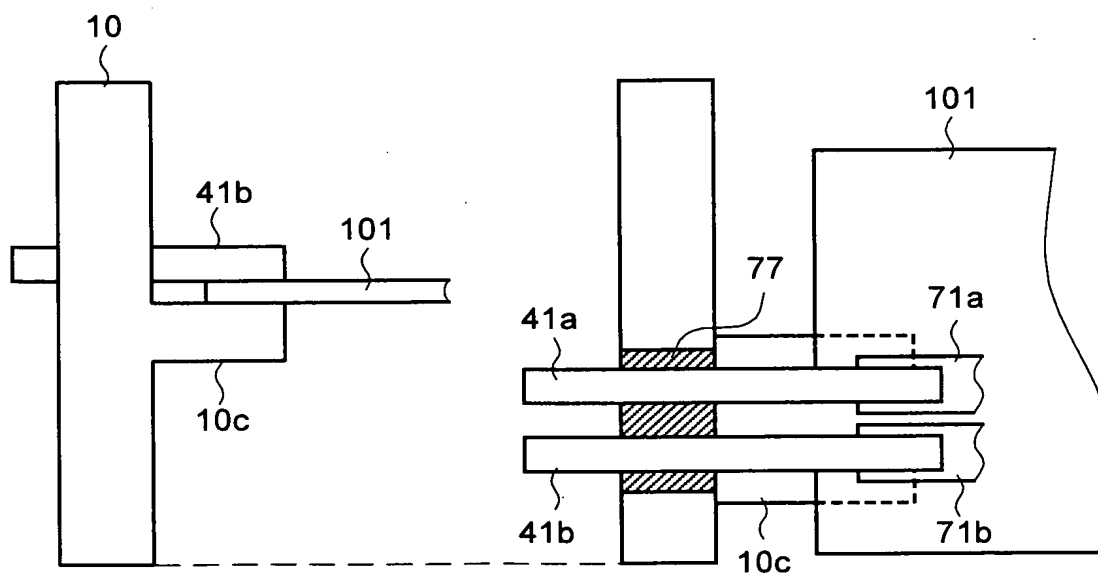
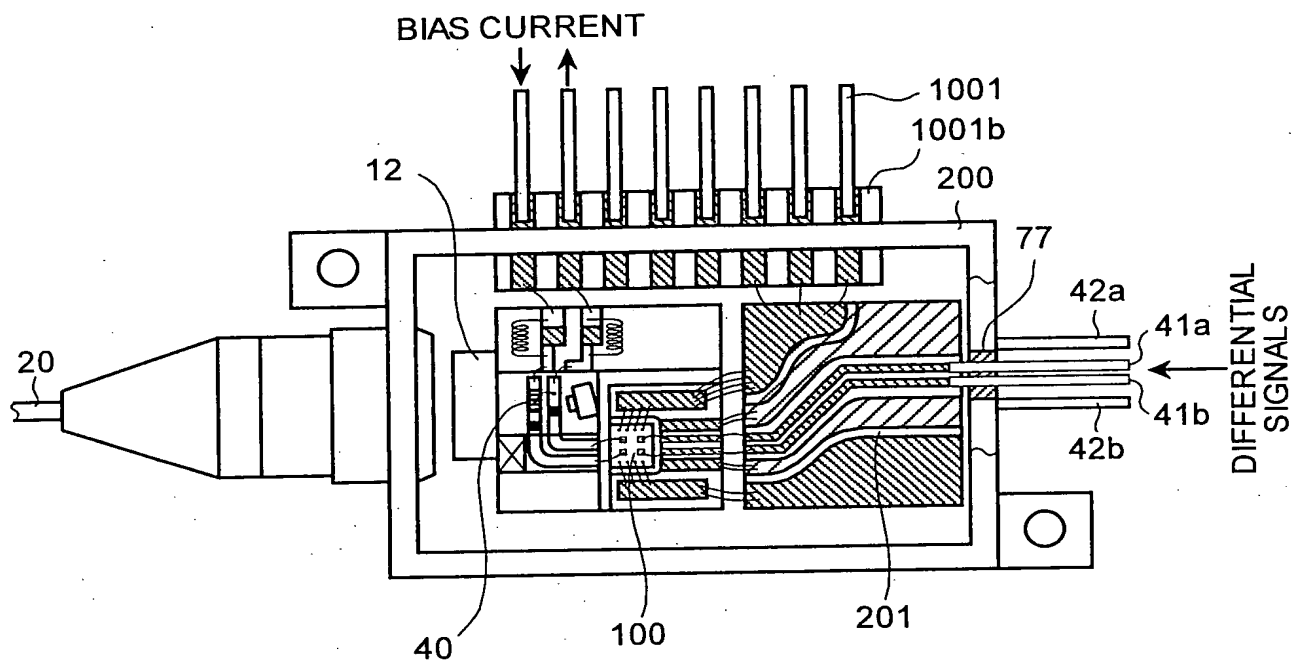
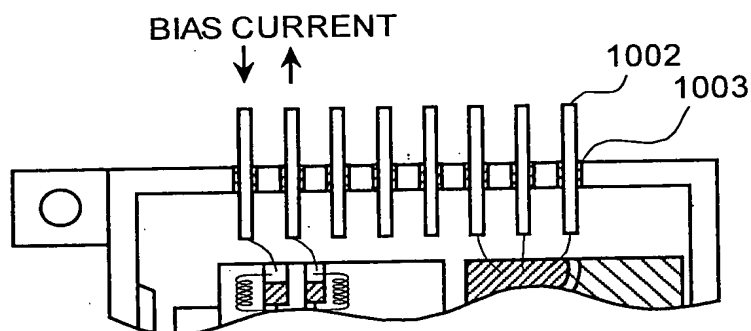


FIG.23



(a)



(b)